31.4 A 22GS/s 5b ADC in 0.13µm SiGe BiCMOS

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Next generation of receivers for 10 to 40Gb/s long-haul optical communication require ADCs to allow the use of DSP-based equalization to correct for signal degradation in the fiber caused by dispersion [1, 2]. For robust operation sampling at twice the data rate is required combined with over 4 ENOB of resolution in the frequency band of interest [3]. To achieve this performance, an ADC using time-interleaved architecture [4] requires periodic calibration using additional circuitry to correct for offset, gain mismatch, and timing skew that result in a large chip area and high power dissipation. The highest speed flash ADCs [1, 2, 5] using both SiGe and InP technologies have been designed with either low sampling rate or resolution. In this paper, a 5b 22GS/s ADC with sufficiently low power dissipation and chip area is presented that could be integrated with the digital circuitry performing the equalization.

The ADC uses flash architecture shown in Fig. 31.4.1. The differential input signal is connected to an array of 17+1 limiting amplifiers with variable offsets. These offsets are controlled with differential currents generated through a resistive ladder and an array of voltage-to-current converters. The outputs of the amplifiers are connected to 32 master-slave flip-flops (MSFF). 16 of them are connected to the output of only one amplifier to generate the first 4 bits directly while the 5^{th} bit is derived through interpolation between the outputs of the adjacent amplifiers using a second set of 16 MSFFs. Since no T/H circuit is used data and clock propagation delays between comparators need to be matched to minimize the clock skew. The thermometer code generated at the output of the comparators is first converted to Gray code followed by a binary encoder.

The accuracy of the converter at high input frequency is largely determined by the performance of the limiting amplifiers shown in Fig. 31.4.2. The input emitter-follower stage beside impedance conversion also performs the level shifting controlled by a differential current. The input DR is 0.64V. It is followed by a broadband limiting amplifier [6] with simulated 16dB gain, 40GHz small signal bandwidth, and 0.5V output swing. This amplifier also prevents kick-back from the clock driving the comparator.

Thermometer to Gray code conversion is performed by summing the appropriate current outputs with alternating polarity [7]. When generating the LSB of the Gray code interconnect parasitics associated with 16 signals could limit the sampling rate therefore, an improved summing circuit is implemented.

To simplify testing, a 6b DAC [8] and linear output buffer with combined 35dB SFDR at 8GHz are integrated with the ADC allowing the reconstruction of the output signal. Digital outputs are also provided after 1:2 divisions. An on-chip VCO and PLL generating the nominal 21.4GHz clock are also integrated with the option to switch to an external clock source. This test circuit is flip-chip mounted directly onto a test circuit board together with a linear amplifier that generates the differential input for the ADC.

INL and DNL are tested using standard code density measurement at 22GS/s sampling rate while driving the ADC with a full-scale 1GHz sine wave input. Figure 31.4.3 shows that both INL and DNL are below 0.5LSB.

The spectrum of the reconstructed signal is analyzed after correcting it for the sin(x)/x roll-off of the DAC and RF signal loss in the cables and connectors. Figure 31.4.4 shows the output spectrum for a 1GHz input signal. The highest spur is the third harmonic of the input signal at -35dB. For flash converters without T/H the main sources of SNDR degradation are clock jitter or skew and distortion caused by signal-dependent delay and finite aperture time [9]. Figure 31.4.5 shows the measured SNDR and SFDR values for a series of input frequencies. These SNDR results indicate that ENOB stays above 4 up to 6GHz then drops to 3.5 at 7GHz input frequency. Clock jitter, that includes variation in the propagation delay between data and clock signals, becomes noticeable between 4 to 5GHz. The slightly higher SNDR degradation over SFDR can be explained by a less than $0.4ps_{rms}$ jitter. For input frequencies above 6GHz spurs-related harmonics dominate SNDR as indicated by the parallel decline of SNDR with SFDR. While most measurements are performed with an external clock source when the internal VCO is turned on SNDR shows no detectable change.

BER is measured by observing the reconstructed output on a sampling oscilloscope in accumulation mode that allows the counting of samples outside of the expected range. Figure 31.4.5 shows the BER for different sampling frequencies for a 1GHz input signal. Error rate increases with sampling frequency and reaches 10^{-4} at 22GS/s which is within the acceptable range for this application. BER performance could be improved by reducing metastability of the comparators by using additional latches.

Figure 31.4.7 shows the die micrograph of the ADC and a summary of the ADC performance. The ADC is fabricated in a 0.13µm SiGe BiCMOS technology. Power dissipation is 3W while operating from a 3.3V supply. The HBTs feature f_t/f_{max} of 150/150GHz while the CMOS transistors are used only in the bias circuits. The layout is designed to ensure that both the data and clock reach the different comparators simultaneously. The comparators are arranged in a U shape around the input data distribution network to minimize clock and data propagation delay.

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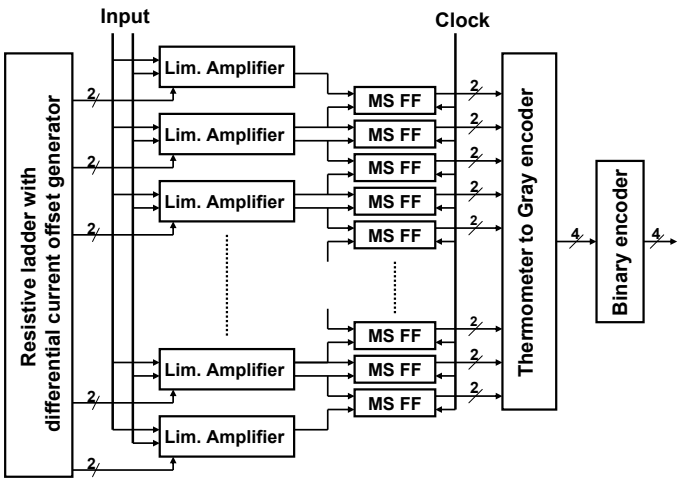

Figure 31.4.1: ADC architecture.

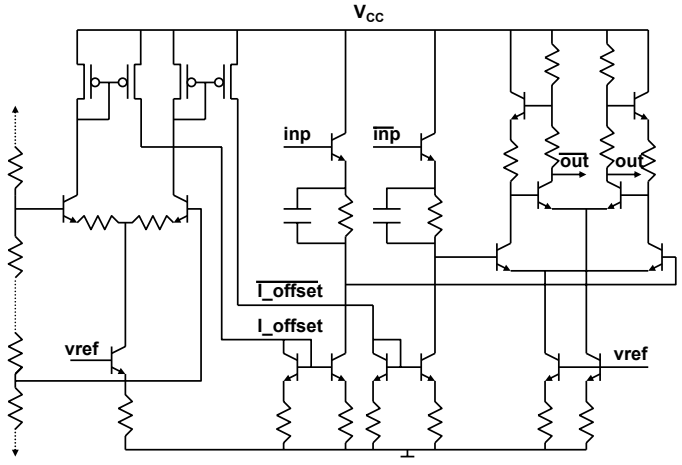

Figure 31.4.2: Schematic of limiting amplifier with offset control.

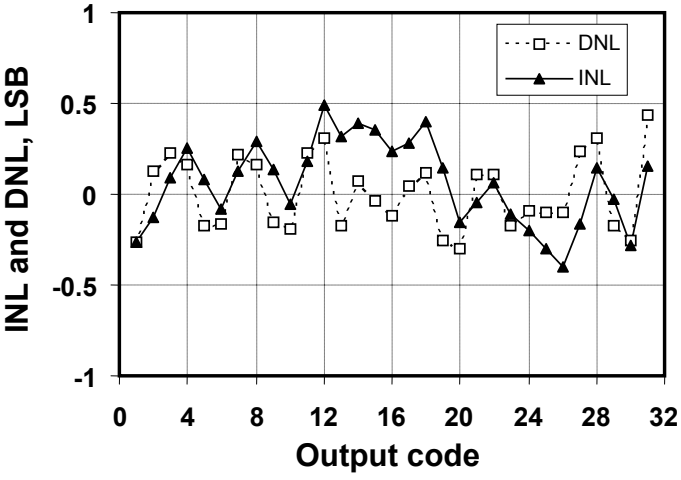

Figure 31.4.3: Measured INL/DNL at f_{in}=100MHz and f_s=22GHz.

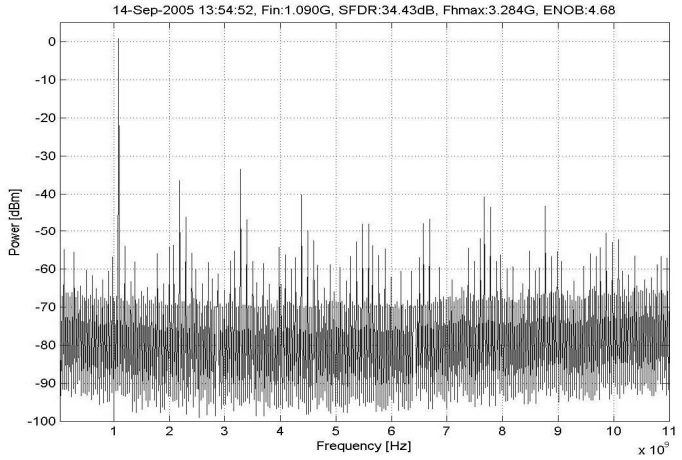

Figure 31.4.4: Measured spectrum for f_{in}=1GHz and f_s=22GHz.

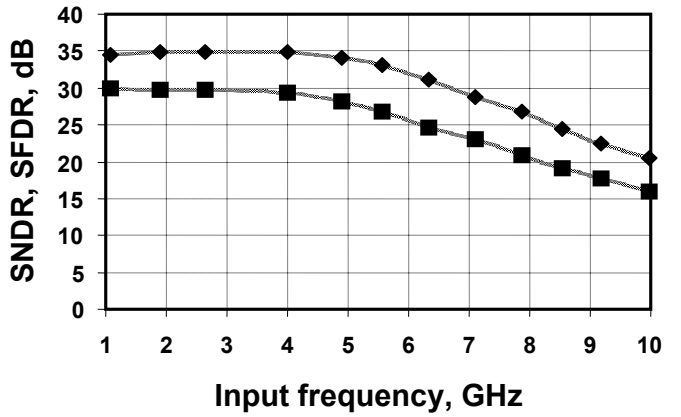

Figure 31.4.5: SNDR and SFDR for different input frequencies.

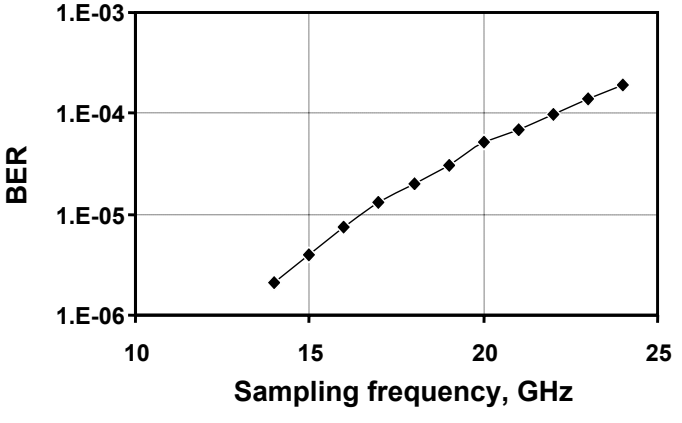

Figure 31.4.6: BER versus sampling frequencies for f_{in}=1GHz.

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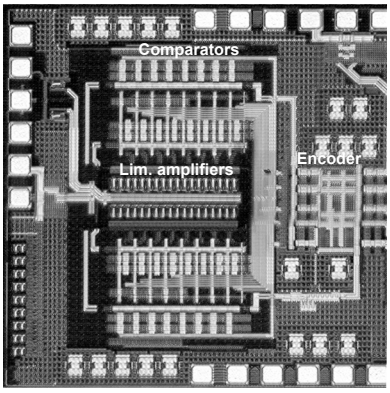

Resolution	5 bits
Conversion rate	22GS/s
Input range	±0.64V
ENOB	4.4 @ 5GHz 3.5 @ 7GHz
SFDR	34dB @ 5GHz 29dB @ 7GHz
Power	3W
Active die area	1.6x1.5mm^2
Process	0.13μm SiGe BiCMOS

Figure 31.4.7: ADC die micrograph and performance summary.

